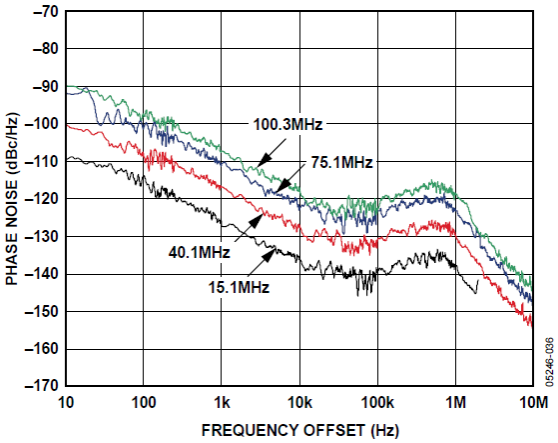
iMS4-L , iMS4-P DDS fundamental specs
Reference – AD9959 data sheet

- **Residual Phase Noise**

Standard iMS4 configuration:
Internal reference clock, (F_{refclk}) = 25MHz
Multiplier (M) = x20 ,
System Clock, (F_{sysclk}) = 500MHz



(Phase noise for AD9959 chip, before downstream amplification).

- **Reference Clock Options**,
  Option to apply an external reference clock (F_{erclk}) input. Please contact Isomet.

PLL Multiplier *	**System Clock**	**Min-Max F_{sysclk} system frequency**	**Min-Max iMS4 output frequency ****
4 ≤ M ≤ 20	$F_{sysclk} = F_{erclk} \times M$	100MHz < F_{sysclk} < 500MHz	40MHz < F_{sysclk} < 200MHz
M < 4, or M > 20 (autosets to M=1)	$F_{sysclk} = F_{erclk}$	0 < F_{sysclk} < 500MHz	0 < F_{sysclk} < 200MHz

* software programmable function of AD9959 DDS chip. Valid range 4 ≤ M ≤ 20.
** maximum iMS4 output frequency = 40% x F_{sysclk}

Default iMS4 settings: VCO gain control bit = 1.
Minimum F_{sysclk} for stable output = 255MHz, Maximum F_{sysclk} = 500MHz
For M=20 (default) this means:
Minimum external reference clock (F_{erclk}) frequency = 13MHz
Maximum external reference clock (F_{erclk}) frequency = 25MHz

Factory option on request: VCO gain bit set = 0.
Minimum F_{sysclk} for stable output = 100MHz . Maximum F_{sysclk} = 160MHz
For M=10 (say) this means:
Minimum external reference clock (F_{erclk}) frequency for stable output = 10MHz
Maximum external reference clock (F_{erclk}) frequency = 16MHz

- **Frequency resolution**

Fundamental output frequency resolution (F_{out}) is given by $F_{out} = FTW \times F_{sysclk} / 2^{32}$

where FTW = frequency tuning word
F_{sysclk} = system clock= 500MHz for standard iMS4

Potential 32-bit resolution = 0.12Hz

Note: At SDK version 1.8.9, the iMS4 firmware is optimized for data throughput. Frequency resolution is currently limited to 16-bit or ~ 2.8KHz.